Corrections approved 11/23/04 PSL

IN THE SPECIFICATION:

Please delete the paragraph beginning on page 7, line 1, and replace with the following new paragraph. Changes from the original paragraph are highlighted.

One particular embodiment of the LBIST domain 160 is conceptually illustrated in FIG. 2. In this-particular embodiment, the LBIST engine 110 comprises an LBIST state machine 210 and a pattern generator 230. The LBIST domain 160 also includes a multiple input signature register ("MISR") 220. The content of the MISR 220 is the LBIST signature 130 in **FIG. 1.** The pattern generator 230 is, more precisely, a pseudo random pattern generator ("PRPG"). In the illustrated embodiment, the LBIST engine 110 is externally configured by a CONFIGURATION signal with a vector count and a PRPG seed for the pattern generator 230. The LBIST engine 110 is configured by a ~~66-bit~~ 65-bit signal received through the testing interface 180 in which 32 bits contain the vector count and 33 bits contain the PRPG seed. Thus, the pattern generator 230 is programmable, as is the LBIST engine 110 as a whole. However, the invention is not so limited and other techniques may be employed for configuring the LBIST engine 110. For instance, these values may be hardcoded or hardwired in alternative embodiments.

Please delete the paragraph beginning on page 9, line 17, and replace with the following new paragraph. Changes from the original paragraph are highlighted.

In accordance with yet another aspect of the invention, the content of the LFSR with which the pattern generator 230 is implemented and the register with which the MISR 220 is implemented are generated using different primitive polynomials to prevent failures disguised by aliasing. The content of the LFSR in the illustrated embodiment is based on the 31-bit primitive polynomial $x^{31} + x^3 + 1$ and the content of the MISR 220 is based on the 32-bit primitive polynomial $x^{32} + x^{18} + x + 1$. If the pattern generator 230 enters an all zero state, the error indicator will be activated and stored in bit *B33* of the MISR 220. In this particular embodiment, the even outputs of the LFSR (bits ~~*B26*~~ *B30* to